LISTING OF THE CLAIMS:

1. (Original) A method of reducing the dislocations present in a SiGe heterojunction bipolar transistor, said method comprising the steps of:

(a) providing a semiconductor substrate having isolation regions formed therein, said semiconductor substrate having an upper surface;

(b) recessing a portion of the isolation regions below the upper surface of said semiconductor substrate so as to provide a recessed isolation surface; and

(c) forming a SiGe layer on the upper surface of the semiconductor substrate as well as said recessed isolation surface, wherein said recessing controls facet formation at edges of the SiGe layer.

2. (Original) The method of Claim 1 wherein said isolation regions are trench isolation regions.

3. (Original) The method of Claim 2 wherein said trench isolation regions are formed by lithography, etching and trench filling.

4. (Original) The method of Claim 3 wherein said trench filling includes deposition of SiO_2.

5. (Original) The method of Claim 1 wherein a patterned dielectric layer is formed on a portion of said isolation regions prior to conducting step (b).

6. (Original) The method of Claim 5 wherein said dielectric is composed of a nitride.

7. (Original) The method of Claim 1 wherein said recessing includes lithography and etching.

8. (Original) The method of Claim 1 wherein after said recessing a patterned dielectric

is formed on a portion of the isolation region that is not recessed.

9. (Original) The method of Claim 1 wherein said SiGe layer is formed by a deposition process selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) and plasma-enhanced chemical vapor deposition (PECVD).

10. (Original) The method of Claim 1 further comprising the steps of:

(d) forming an insulator on said SiGe layer;

(e) providing an opening in said insulator so as to expose a portion of said SiGe base region;

(f) forming an emitter material on said insulator and in said opening so as to contact said SiGe base region; and

(g) patterning said emitter material and said insulator so as to form a patterned emitter and a patterned insulator on said SiGe base region.

Claims 11-19 (Cancelled)